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Author Ming-Chang Lee
Author's Email Address No Public.
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Abstract
The Viterbi algorithm, widely used in digital communication systems, is known to be an efficient method for the realization of maximum likelihood decoding of convolution codes. Convolution codes are widely used in many communication systems due to their excellent error control performance.
In this thesis, a most-significant-bit (MSB)-first ACS unit is used to implement a high speed Viterbi decoder. The ACS unit is the main bottleneck on the decoding speed of a Viterbi decoder. By balancing the settling time of different paths in the ACS unit, the length of the critical path is reduced as close as possible to the iteration bound in the ACS unit. We supply a flexible IP implementation of channel decoding to easily adjust code rate and memory progression variable. With the help of our IP modules, the chip design time can be reduced efficiency.
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